REMARKS

This Application has been carefully reviewed in light of the Final Action issued September 28, 2007. Claims 1-24 are pending in this Application. In order to advance prosecution of this Application, Claims 1, 3, 4, 13, 15, and 16 have been amended. Applicant respectfully requests reconsideration and favorable action for this Application.

Claims 1 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chuah, et al. in view of Altera and further in view of Duling III, et al. Independent Claims 1 and 13 have been amended to include the features of Claims 3 and 15 respectively. Independent Claims 1 and 13 recite in general an ability to receive a time division multiplexed data stream at an ingress end from an optical carrier, divide said data stream into a set of fixed sized packets, add a service header to each of said packets, and add an additional header on top of said service header in accordance with MPLS protocols, and use the service header to include a structure pointer to indicate whether a header byte indicating a start of a synchronous payload envelope is present within a packet with said structure pointer indicating a location of said header byte in said packet. The Examiner readily admits that the Chuah, et al. patent, the Altera paper, and the Duling III, et al. patent fail to teach a structure pointer to indicate whether a header byte indicating a start of a synchronous payload envelope is present within a packet with said structure pointer indicating a location of said header byte in said packet. With respect to the Armitage paper, there is no disclosure whatsoever in the cited portion therein that it can indicate whether a header byte in a synchronous payload envelope is present within a packet as provided in Claims 1 and 13. The cited portion of the Armitage paper

merely refers to defining MPLS forwarding for a range of link layer technologies such as SONET/SDH. Nothing in this citation relates at all to indicating whether a header byte is present in a packet and its location within the packet. The Examiner has failed to show that the cited portion, or any other portion, of the Armitage, et al. paper teaches the claimed structure pointer. Therefore, Applicant respectfully submits that Claims 1 and 13 are patentably distinct from the proposed Chuah, et al. - Altera - Duling III, et al. - Armitage combination.

Claims 2-12 and 14-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chuah, et al. in view of Altera and Duling III, et al. and further in view of Armitage. Independent Claim 1, from which Claims 2-12 depend, and Independent Claim 13, from which Claims 14-24 depend, have been shown above to be patentably distinct from the proposed Chuah, et al. - Altera - Duling III, et al. combination. Moreover, the Armitage paper does not include any additional disclosure combinable with the Chuah, et al. patent, the Altera paper, or the Duling III, et al. patent that would be material to patentability of these claims.

With respect to Claims 2 and 14, the S-bit of the Armitage paper merely indicates the final stack entry before the original packet and does not indicate a break in the data stream according to an alarm bit as required in Claims 2 and 14.

With respect to Claims 3 and 15, none of the cited references to disclose the use of negative and positive justification bits in the service header of a packet to indicate whether said synchronous payload envelope includes a negative stuff byte or a positive stuff byte.

With respect to Claims 4 and 16, the cited portion of the Armitage paper fails to mention anything about providing an indication that a header byte is not present in a packet as provided in Claims 4 and 16. The cited portion of the Armitage paper merely discusses prepending an MPLS frame with one or more MPLS label entries and popping the label at egress and forwarding the packet based on the popped label.

With respect to Claims 5 and 17, there is no mention of an ability to record a stuffing time difference in a service header in the cited portion of the Armitage paper as is provided in Claims 5 and 17. The cited portion of the Armitage paper merely discusses the generic MPLS frame structure with without a word about stuffing time differences.

With respect to Claims 6 and 18, the Examiner cites a single word from the Armitage paper to support four of the features of Claim 6 and 18. However, this single word fails to disclose the specific features provided by Claims 6 and 18. Moreover, the Examiner cites the TTL field of the Armitage paper that prevents a MPLS packet from looping. By contrast, Claims 6 and 18 recite generating a positive or negative justification indicator in response to a data average comparison to a threshold in order to determine whether one more or one less byte is sent. The Armitage paper fails to disclose this technique of sending one more or one less byte.

With respect to Claims 7 and 19, the cited portion of the Armitage paper fails to disclose an ability to locate at least one header byte in said set of packets and measure all bytes between two header bytes as required by Claims 7 and 19. The Examiner merely cites the forwarding treatment of packets by the Armitage paper using a single index lookup into a switching table. There is no mention of measuring bytes between two header bytes as provided by Claims 7 and 19.

With respect to Claims 8 and 20, the Armitage paper fails to disclose the insertion of a dummy packet when a packet in a sequence is missing. The portion of the Armitage paper cited by the examiner merely refers to prepending a label entry to a MPLS frame and no capability for dummy packet insertion as provided in Claims 8 and 20.

With respect to Claims 9 and 21, the Examiner cites the ability provided by the Armitage paper to include a TTL field in the packet that is decremented to allow discarding of the packet and prevent the packet from looping. However, this TTL field has no relationship to any packet sequencing nor does it allow for discarding of out of sequence packets as provided in Claims 9 and 21.

With respect to Claims 10 and 22, the Examiner asserts that the features of these claims are inherent to the SONET process. The Examiner provides no basis for this assertion and has not shown that the SONET process is capable of performing the features of Claims 10 and 22.

With respect to Claims 11 and 23, the portion of the Armitage paper cited by the Examiner merely mentions building a concatenated sequence of appropriate label mappings in the switching tables of LSRs along the desired path. The Armitage paper does not provide any capability for checking that packets are sequentially present let alone establishing an in-frame condition upon receiving a set of packets in sequence as required by Claims 11 and 23.

With respect to Claims 12 and 24, the Examiner cites the Armitage paper for its disclosure of 3 additional bits for experimentation to indicate scheduling disciplines. However, the Armitage paper provides no details as to what is meant by scheduling disciplines and fails to disclose anything about

the claimed in-frame condition let alone a capability to determine whether it is valid as provided in Claims 12 and 24.

As shown above, each of dependent Claims 2-12 and 14-24 are patentably distinct from the cited art based on their dependence to Independent Claims 1 and 13 as well as providing features not disclosed on the proposed Chuah, et al. - Altera - Armitage combination. The Examiner has failed to respond to Applicants remarks pointing out the deficiencies of the Armitage, et al. paper with respect to the dependent claims. Therefore, Applicant respectfully submits that Claims 2-12 and 14-24 are patentably distinct from the proposed Chuah, et al. - Altera - Duling III, et al. - Armitage combination.

This Response to Examiner's Action is necessary to address the new grounds of rejection and newly cited art introduced by the Examiner and to address the Examiner's failure to respond to deficiencies in the prior art with respect to the dependent claims. This Response to Examiner's Final Action could not have been presented earlier as the Examiner did not address the deficiencies of the prior art with respect to the dependent claims and has only now introduced the new grounds of rejection and newly cited art.

CONCLUSION

Applicant has now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests reconsideration and full allowance of all pending claims.

The Commissioner is hereby authorized to charge any amount required or credit any overpayment to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
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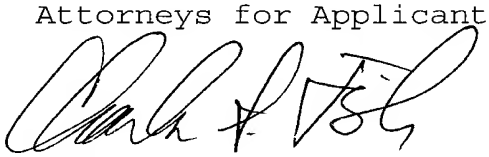
Attorneys for Applicant



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